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EXAMINER	
RIZZUTO, KEVIN P	

ART UNIT	PAPER NUMBER
2183	

DATE MAILED: 01/24/2006

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	09/974,924	MAYER, ALBRECHT	
	Examiner	Art Unit	
	Kevin P. Rizzuto	2183	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *11/16/06*.

2a)☒ This action is **FINAL**. 2b)☐ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-17* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-17* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☐ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

Detailed Action

1. Claims 1-17 have been examined.

Papers Submitted

2. It is hereby acknowledged that the following papers have been received and placed on record in the file: amendment received 11/16/2005.

Withdrawn Objections

3. Applicant, via amendment, has overcome the objection to Claim 10 previously set forth. Therefore, the objection has been withdrawn.

Maintained Claim Rejections – 35 USC § 103

4. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

5. Claims 1-7, 10-15 and 17 are rejected under 35 U.S.C. 103(a) as being unpatentable over Harrison, EP 0 455 946 A2.

6. Regarding claim 1, Harrison, has taught a programmable unit, comprising:

a. At least one program operation unit for running a program

[Processor 16 (PO 16), fig. 1 and col. 3, lines 11-19]

b. A stopping device (bus monitor 12, figures 1 and 2) connected to said program operation unit said stopping device stopping the running of the program by said program operation unit [Col. 3, line 42 to col. 4, line 24, col. 8, line 55 to col. 9, line 16 and figure 4.]

c. Other components [P1-P7, fig. 1] connected to said stopping device said stopping device also issuing a stop command causing said other components to be stopped, in addition to stopping said program operation unit with which said stopping device is associated: [Col. 3, line 42 to col. 4, line 24, col. 8, line 55 to col. 9, line 16 and figure 4.]

d. And said other components including at least one further program operation unit or at least one peripheral [P1-P7, fig. 1], said stopping command being selectively provided from said stopping device to said other component if said other component is said further program operation unit [Col. 3, line 42 to col. 4, line 24, col. 8, line 55 to col. 9, line 16 and figure 4.]

e. And said stop command being directly provided from said stopping device to said other component if said other component is a peripheral: [Col. 3, line 42 to col. 4, line 24, col. 8, line 55 to col. 9, line 16 and figure 4.]

f. Examiner notes that the claim language only requires the other components to be *either* a further program operation unit *or* a peripheral, *not both.* However, The American Heritage Dictionary of the English Language, 4th Ed defines peripheral as, "An auxiliary device, such as a

printer, modem, or storage system, that works in conjunction with a computer." It then defines auxiliary as, 1. Giving assistance or support; helping." A processor within a multiprocessor system is a peripheral to the other processors, and the other processors are peripherals to the processor, since each works in conjunction with a computer giving assistance or support to carry out data processing. Therefore, any of the processors, P1-P7 could be considered either a peripheral or a program operation unit.

7. However, Harrison has not taught wherein said stopping device is located on the same chip as said program operation unit.

8. It would have been obvious to one of ordinary skill in the art at the time the invention was made to integrate the bus monitor 12 and the PO 16 onto a single chip since it has been held "that the use of a one piece construction instead of the structure disclosed in [the prior art] would be merely a matter of obvious engineering choice." [In re Larson, 340 F.2d 965, 968, 144 USPQ 347, 349 (CCPA 1965)]

9. Given the similarities between the claims, the arguments as stated for claim 1 are also applicable to claim 11.

10. Regarding claim 2, Harrison has taught the programmable unit according to claim 1, wherein said other components [P1-P7, fig.1] include at least one further program operation unit and said stopping device able to stop said further program operation unit which is not associated with said stopping device. [Col. 3, line 42 to col. 4, line 24, col. 8, line 55 to col. 9, line 16 and figure 4.]

11. Regarding claim 3, Harrison has taught the programmable unit of claim 2, wherein said other components [P1-P7, fig. 1] which can be stopped by said stopping device include units which are connected to and cooperate with said program operation unit and said further program operation unit: [Col. 3, line 42 to col. 4, line 24, col. 8, line 55 to col. 9, line 16 and figure 4.]

12. Regarding claim 4, Harrison has taught the programmable unit of claim 3, wherein said units are stopped by said stopping device later in time than said program operation unit and said further program operation unit: [The processors (P1-P7) can be selectively stopped, depending on the settings within bus monitor 12. The settings are alterable, i.e., the bus monitor can be set up to issue stop commands to certain processors at one point during processing, then the set-up can be altered so that different processors are issued the stop command. [Fig. 5, and col. 9, lines 17-35] Therefore, some units (e.g., PO 3 and 4) can be initially not given the stop command upon a first breakpoint. Then, the bus monitor 12 can be reconfigured so that upon another breakpoint (later in time), the units (PO 3 and 4) will be issued a stop command.]

13. Given the similarities between the claims, the arguments as stated for claim 4 are also applicable to claim 12.

14. Regarding claim 5, Harrison has taught the programmable unit of claim 4, including at least one bus connected between said other components [Figure 1]

15. Given the similarities between the claims, the arguments as stated for claim 5 are also applicable to claim 13.

16. Regarding claim 6, Harrison has taught the programmable unit of claim 5, including bus interfaces and each of said bus interfaces is connected to one of said program operation unit and said further program running unit and to said bus: The program operation unit [P0] and further program running unit [Any of [P1-P7]: Each of the processors [P0-P7] is connected to a bus as shown in figure 1, [Shared-Memory Bus 15]. Interface is defined as, "A surface forming a common boundary between adjacent regions, bodies, substances, or phases. 2. A point at which independent systems or diverse groups interact. 3. *Computer Science* a. The point of interaction or communication between a computer and any other entity, such as a printer or human operator." (The American Heritage College Dictionary, 4th Edition) Therefore, since the bus is connected to both the program operation unit and said further program running unit, there is an interface present at the connection point, in which both the bus and the program operation unit or said further program unit are connected.

-Said program operation unit and said further program operation unit function as bus masters: [Each of the processors (P0-P7) operate as bus masters since each has memory controller. When a processor has access to the shared bus to communicate with the shared memory (Read or Write), it is functioning as a bus master. Col. 3, lines 20-34, figure 1.]

17. Harrison teaches where the bus monitor 12 selectively issues the stop command (an interrupt) to processors (P0-P7) and wherein the interrupts is assigned a priority level by the bus monitor 12 as well. However, the priority level of the stop command is not specifically assigned, it is only stated that "the

bus monitor 12 is configured to identify which processors are to be interrupts and an interrupt level to be used." (Col. 4, lines 12-14). Therefore, Harrison does not explicitly teach where said units are stopped only when said bus masters and said bus interfaces have no more data to output and/or are no longer waiting for already requested data or data that is still to be requested.

18. One of ordinary skill in the art would have recognized to set the interrupt level in such a way as to allow the current pending transactions to be completed by the processor so as to allow the pending instructions to be completed before probing of the processors is begun. This will allow a known architected state to be debugged, as opposed to a possibly unknown state, which is what may occur when an interrupt is given a higher priority than the pending bus/memory operations. Therefore, it would have been obvious to one of ordinary skill in the art to have a low-enough interrupt level associated with the stop command (breakpoint interrupts) so as to allow the bus masters and bus interfaces to wait for pending operations to be completed before the interrupt occurs.

19. Given the similarities between the claims, the arguments as stated for claim 6 are also applicable to claim 14.

20. Regarding claim 7, Harrison has taught the programmable unit according to claim 5, wherein said bus includes a first bus part, a second bus part and a bus bridge connecting said first bus part to said second bus part: [Figure 1. Each vertical line portion of Shared – Memory Bus 15 is a "bus part". The horizontal line portion of Shared – Memory Bus 15 is the "bus bridge" connecting said first bus part to said second bus part.]

21. Harrison teaches where the bus monitor 12 selectively issues the stop command (an interrupt) to processors (P0-P7) and wherein the interrupts is assigned a priority level by the bus monitor 12 as well. However, the priority level of the stop command is not specifically assigned, it is only stated that "the bus monitor 12 is configured to identify which processors are to be interrupts and an interrupt level to be used." (Col. 4, lines 12-14). Therefore, Harrison does not explicitly teach wherein said units are stopped only when said bus bridge has no more data to pass on.

22. One of ordinary skill in the art would have recognized to set the interrupt level in such a way as to allow the current pending transactions to be completed by the processor so as to allow the pending instructions to be completed before probing of the processors is begun. This will allow a known architected state to be debugged, as opposed to a possibly unknown state, which is what may occur when an interrupt is given a higher priority than the pending bus/memory operations. Therefore, it would have been obvious to one of ordinary skill in the art to have a low-enough interrupt level associated with the stop command (breakpoint interrupts) so as to allow the bus masters and bus interfaces to wait for pending operations to be completed before the interrupt occurs.

23. Given the similarities between the claims, the arguments as stated for claim 7 are also applicable to claim 15.

24. Regarding claim 10, Harrison has taught the programmable unit of claim 1, wherein said stopping device is an on-chip debug support module. [It is inherent that the stopping device (bus monitor 12) is designed/made on a chip

because it contains hardware and logic as shown in figure 2. Harrison discloses there the bus monitor device is used for debugging and monitoring. [Col. 3, line 42 to col. 4, line 39]

25. Given the similarities between the claims, the arguments as stated for claim 10 are also applicable to claim 17.

26. Claims 8, 9 and 16 are rejected under 35 U.S.C. 103(a) as being unpatentable over Harrison, EP 0 455 946 A2, and further in view of Wen et al., U.S. Patent 5,956,514, herein referred to as Wen.

27. Regarding claim 8, Harrison has taught the programmable unit of claim 1, but does not give a thorough disclosure of the restarting of the application on the parallel processors (P0-P7). Harrison only states that the Processor 16 (P0) runs the debugging program and it issues a command to resume execution of the application when the debugging is completed. Therefore, processor 16 (P0) is the master processor, and the others are slaves.

28. However, Harrison fails to teach wherein after a stopped state of components of the programmable unit which have been stopped is cancelled, said units recommence operation before said program operation unit and said further program operation unit recommence operation.

29. Wen teaches wherein after a breakpoint, and debugging, the Master processor can issue a restart command [unhold_cpu()] to individual slave processors. The restart command can either indicate to start the application over from the beginning or to resume at the point from which it was interrupted at. This allows a greater degree of flexibility for the programmer, because it is

possible to selectively restart processors. [Col. 6, lines 41-64 and figure 1] This is similar to Harrison's teaching for selectively issuing the stop commands, which has the of increased flexibility for debugging purposes. Adding this feature to Harrison would cause the P0 processor to cause the "units" to recommence processing before the P0 processors does, and also at different times from each other. Therefore, the restarting command would cause the "units" to recommence operation before said program operation unit and said further program operation unit.

30. It would have been obvious to one of ordinary skill in the art to use the teachings of Wen, wherein slave processors can be selectively resumed, since it would increase the flexibility of the debugging process.

31. Regarding claims 9 and 16, given the similarities between claim 8 and claims 9 and 16, the arguments as stated for claim 8 are also applicable to claims 9 and 16.

Response to Arguments

1. Applicants arguments filed on 11/16/05 have been fully considered but they are not persuasive.

2. Applicant argues the novelty/rejection of claim 1.

"Contrary to Applicant's invention of claim 1, Harrison neither teaches, nor suggests, **a stopping command, once generated by the stopping device, being selectively provided from the stopping device to another component if the other component is a further program operation unit.**"

"As such, in order to teach or suggest the limitations of Applicant's claim 1, Harrison must disclose that the bus monitor 12 of Harrison (analogized in the Office Action to the Applicant's 'stopping device') **issues a stop command and then**

selectively provided the stopping command to at least one of the further program operation units (i.e., processors p1-p7). However, the Harrison reference fails to teach or suggest among other limitations of Applicant's claim, that a stopping device actually issues a stopping command to another component, and then only selectively provides the stopping command to the other component, which is a program operation unit.

Rather, in Harrison, **every time a stopping command is issued** for an intended processors p1-p7, **the intended processor p1-p7 is stopped**. See, for example, col. 7 of Harrison, lines 19-26 (all processors **stopped** if any processor tries to write to a shared memory location for variable X); col. 7 of Harrison, line 57 (all processors **stopped** if trace memory is full); and col. 7 of Harrison, lines 40-42 (a specified processor is stopped if the specified processor tries to write to a shared memory location for variable X). In all of the above examples, the processors p1 – p7 are **all** operating as **program operation units** and **all are stopped by the bus monitor 12 of Harrison. Harrison** does not teach or suggest that, **when a stopping command is issued by the stopping device, it may be selectively** provided to a program operation unit, as required by Applicant's claim 1.

In the Office Action, it is alleged on page 3, paragraph d, that Applicant's invention of claim 1, including the stopping command being selectively provided, is disclosed in Harrison in col. 3, line 43-col. 4, line 24, col. 8, line 55 – col. 9, line 16 and figure 4. However, Applicant respectfully disagrees. Applicant has reviewed the cited portions of Harrison and has not found such a teaching. It is believed that, perhaps, the Office Action was attempting to point to col. 9 of Harrison, lines 5-10 (shown graphically in Fig. 4) as allegedly teaching selectively stopping a processor. Col. 9 of Harrison, lines 5-10, states:

> When a match is found between a detected event and the event defined in the event comparator 30, the event may either be logged into the trace memory in step 61 or an interrupt may be produced, depending on the quality and nature of the detected event. [emphasis added by Applicant]

Although the cited portion of Harrison describes **selectively producing an interrupt**, it neither teaches or suggests **affirmatively producing an interrupt and selectively providing the produced interrupt to a further program operation unit**, as required by Applicant's claim 1."

3. These arguments are not found persuasive for the following reasons:

a. To clarify, applicant's attention is first directed towards the claim limitations in question, which are recited below:

i. "[S]aid stopping device issuing a stop command causing said other components to be stopped...said stopping command being selectively provided from said stopping device to said other component"

b. In the portions that were previously cited, Harrison teaches, "The bus monitor 12 is configured to identify which processors are to be interrupted" (col. 4, lines12-14) and "[w]hen and interrupt is issued, the interrupt is conveyed via the control bus interface 29 to the appropriate processors in step 62" (col. 9, lines13-16). Therefore, it is shown wherein the stopping command is selectively issued "to the appropriate processors" and that the "bus monitor 12 is configured to identify which processors are to be interrupted" (stopped), and thus, the claimed limitations are taught by Harrison. Furthermore, Applicant has stated, "See, for example, col. 7 of Harrison, lines 19-26 (all processors **stopped** if any processor tries to write to a shared memory location for variable X); col. 7 of Harrison, line 57 (all processors **stopped** if trace memory is full); and col. 7 of Harrison, lines 40-42 (a specified processor is stopped if the specified processor tries to write to a shared memory location for variable X)", which shows in some instances, all processors are stopped, while in others, only some selected processors are stopped.

c. Applicant appears to be arguing that the claim requires two ordered steps, that is, one in which the stop command is issued, and then later in time, the stop command is selectively applied (and possibly by some other device (not claimed)). However, as previously stated, the claimed limitations are taught by Harrison. The claim states, "**said stopping command being selectively provided <u>from said stopping device</u>** to said other component if said other component is said further program

operation unit." (Emphasis added by Examiner) The claim calls for one stopping device, which issues a stopping command and does so in a selective manner. There are no limitations in the claim which necessitate the stopping command is issued by said stopping device and then at a later moment in time, it is selectively applied, as Applicant appears to be arguing. In fact, the recited claim limitation implies that it issuing and selective application of the stopping command are concurrently performed, since it is one single device that issues the stopping command and said stopping command is "selectively provided from said stopping device". Furthermore, in response to applicant's argument that the references fail to show certain features of applicant's invention, it is noted that the features upon which applicant relies (i.e., "**issues a stop command and then selectively provides the stopping command to at least one of the further program operation units**" (page 13 of 18) and "**a stopping command, once generated by the stopping device, being selectively provided from the stopping device to another component if the other component is a further program operation unit**" (page 11 of 18)) are not recited in the rejected claim(s). Although the claims are interpreted in light of the specification, limitations from the specification are not read into the claims. See *In re Van Geuns*, 988 F.2d 1181, 26 USPQ2d 1057 (Fed. Cir. 1993).

4. Applicant argues the novelty/rejection of claim 1.

"More particularly, the Harrison reference discloses a multiprocessor computer including a plurality of parallel processors p0-p7 (see Fig. 1 of Harrison). The parallel

processors of Harrison are used for running programs, as stated in col. 4 of Harrison, lines 22-27, which states:

> **The application running in processors 16-23 will be halted during breakpoints which are detected by the bus monitor, and a symbolic debugging may be carried out by invoking the debugging program running in processor 15 on each of these executing processors 15 through 23.** [emphasis added by Applicant]

"As can be seen, in the Harrison reference, the processors p1-p7 (i.e., processors 17-23 of Fig. 1 of Harrison), would be analogous to a 'further program operation unit' component of Applicant's claims. That the processors p1-p7 of Harrison operate at least as further program operation units is conceded on page 4 of the Office Action (i.e., 'Therefore, any of the processors, P1-P7 could be considered either a peripheral or a program operation unit"). However, Applicant respectfully disagrees with the statement made in the Office Action that the processors p1 – p7 of Harrison could be peripherals or a program operation unit. Rather, Applicant believes that, as defined by the specification of the instant application and that of Harrison, the processors p1 – p7 can only be considered to be further program operation units, when applied to Applicant's claims. Applicant defines program operation units as being **for running programs**. Applicant defined peripherals as units being used in programmable units, in addition to one or more program running units, to cooperate with them. More particularly, Applicant's specification, in paragraph [0029], clearly defines **peripheral units** as:

> The peripheral units P1 and P2 are, for example, A/D converters, timers, DMA controllers or other units, which can be used in programmable units in addition to one or more program running units, and cooperate with them.

As such, as defined by Applicant's specification, and as clearly used in the claims, program running units, **units running a program**, are precluded from being peripherals.

The processors, p1 – p7 of Harrison, are program running units that are running a program (see, col. 4 of Harrison, lines 22-27), and, as such, **as defined by the specification of the instant application**, are acting as **further program operation units** for purposes of Applicant's claims.

Applicant's application clearly defines, both in the specification **and in the claims**, peripheral units and program operation/running units as two different things. Peripherals, by their very definition in the instant specification, cooperate with one or more program running units, **but are not program running units**. The processors p1 – p7 of the Harrison reference are **clearly program operation units** as define in the instant application, and **not peripheral units**."

5. These arguments are not found persuasive for the following reasons:

d. To clarify, applicant's attention is directed towards the language of claim 1. The claim recites the limitation, "said other components including at least one further program operation unit ***or*** at least one peripheral." The limitation clearly uses alternative language which does not necessitate the claimed "other components" to include a peripheral. That is, it is not necessary for Harrison to teach a "peripheral" for it to anticipate the limitations of claim 1. Harrison teaches wherein the "other components" include "at least one further program operation unit" and therefore, the claim limitations in question are taught.

e. Regardless of whether or not a "peripheral" is claimed, Harrison teaches said "other components" include "at least one peripheral." The below portion is extracted from the maintained rejection of claim 1 above:

> i. Examiner notes that the claim language only requires the other components to be *either* a further program operation unit *or* a peripheral, *not both*. However, The American Heritage Dictionary of the English Language, 4th Ed defines peripheral as, "An auxiliary device, such as a printer, modem, or storage system, that works in conjunction with a computer." It then defines auxiliary as, 1. Giving assistance or support; helping." A processor within a multiprocessor system is a peripheral to the other processors, and the other processors are peripherals to the processor, since each works in conjunction with a computer giving assistance or support to carry out data processing. Therefore, any of the processors, P1-P7 could be considered either a peripheral or a program operation unit.

f. Applicant has argued that "peripheral" and "program operation/running units" are clearly defined in both the specification and

claims. Examiner finds this argument unpersuasive for the following reasons:

ii. The specification does not clearly define peripheral units. The portion of the specification cited by Applicant, that allegedly clearly defines "peripheral" does not, in fact, provide a clear definition. The specification states:

> ***(1)*** "The ***peripheral units*** P1 and P2 ***are***, ***for example***, A/D converters, timers, DMA controllers ***or other units***, ***which can be used in programmable units in addition to one or more program running units, and cooperate with them."***

iii. To begin, peripheral units are defined using the phrase, "are, for example" and then lists multiple options including "or other units". This is not a clear definition, as the metes and bounds of "other units" are not inherently known or provided. Furthermore, the "for example" is not limiting the definition to only those options listed after. It is unclear what other examples would fit Applicant's intended use of the term peripheral. Furthermore, it is unclear if the following line, "which can be used in programmable units in addition to one or more program running units, and cooperate with them," is directly associated with the examples listed or the "peripheral units".

iv. Furthermore, the processors (p1-p7) of Harrison meet Applicant's alleged "clear" definition. The processors (p1-p7) are

"**other units**" and they "**can be used in programmable units in addition to one or more program running units**", as they are in a multiprocessor system (programmable unit) along with other program running units (the other processors p1-p7). Lastly, the processors (p1-p7) cooperate with each other, as they are in a multiprocessor system. Nowhere in the definition of peripheral, is the ability to run programs precluded, yet this is what Applicant has asserted.

v. In conclusion, neither the specification nor the claims provide a clear definition of peripheral. Furthermore, the processors (p1-p7) fit both the common dictionary definition of peripheral and the Applicant's broad definition of peripheral. See also MPEP 2111 [R-1] "Claim Interpretation; Broadest Reasonable Interpretation" and MPEP 2111.01 [R-3] "Plain Meaning" for further details regarding claim interpretation and definitions.

6. Applicant arguments regarding the novelty/rejection of claim 11 are substantially the same as those regarding claim 1, and therefore, have been found unpersuasive for the reasons stated above.

Conclusion

7. **THIS ACTION IS MADE FINAL.** Applicant is reminded of the extension of time policy as set forth in 37 CFR 1.136(a).

The following is text cited from 37 CFR 1.111(c): In amending in reply to a rejection of claims in an application or patent under reexamination, the applicant or patent owner must clearly point out the patentable novelty which he or she thinks the claims present in view of the state of the art disclosed by the references cited or the objections made. The applicant or patent owner must also show how the amendments avoid such references or objections.

A shortened statutory period for reply to this final action is set to expire THREE MONTHS from the mailing date of this action. In the event a first reply is filed within TWO MONTHS of the mailing date of this final action and the advisory action is not mailed until after the end of the THREE-MONTH shortened statutory period, then the shortened statutory period will expire on the date the advisory action is mailed, and any extension fee pursuant to 37 CFR 1.136(a) will be calculated from the mailing date of the advisory action. In no event, however, will the statutory period for reply expire later than SIX MONTHS from the mailing date of this final action.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Kevin P Rizzuto whose telephone number is (571) 272-4174. The examiner can normally be reached on M-F, 8-4:30.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Eddie Chan can be reached on (571) 272-4162. The fax phone number for the organization where this application or proceeding is assigned is 703-872-9306.

KPR

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SUPERVISORY PATENT EXAMINER
TECHNOLOGY CENTER 2100